JEDEC STANDARD

Description of a 3.3 V, Zero Delay Clock Distribution Device Compliant with JESD21-C, PC133 Registered DIMM Specification

JESD82-5

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DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH JESD21-C, PC133 REGISTERED DIMM SPECIFICATION

(Formerly JEDEC Board Ballot JCB-02-53, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines pinout, functionality, DC and AC interface parameters, and test loading for the functions known as the '2509 and '2510. The scope of the specification is restricted to those parameters critical to operation with the PC133 Registered DIMM applications.

The purpose is to provide a standard for a zero delay PLL based clock distribution device compatible with the requirements of the PC133 Registered DIMM specification operating with a nominal supply voltage (V_{DD}) of 3.3 V.

2 Terms and definitions

PC133: A JEDEC designation for systems with a 133 MHz Front Side Bus using SDRAM main memory technology running at a clock frequency of a 133 MHz.

3 Device standard

3.1 Description

The '2509/'2510 are high performance, low skew, low jitter, zero delay clock buffers designed for high fan out applications. Phase and frequency alignment between the CKIN input and Y_n outputs are achieved through an internal PLL. The device is designed to operate over a 3.0 V to 3.6 V supply voltage range.

The '2509 has one feedback output (FBOUT) and nine standard outputs arranged as one bank of five outputs and one bank of four outputs. The '2510 has one feedback output and one bank of ten standard outputs. Each output is a logical AND of the output of the PLL and the respective OE signal of that bank. When the OE signal is asserted low all outputs of that bank are forced into a LOW state. The FBOUT signal is not disabled by the OE signal.

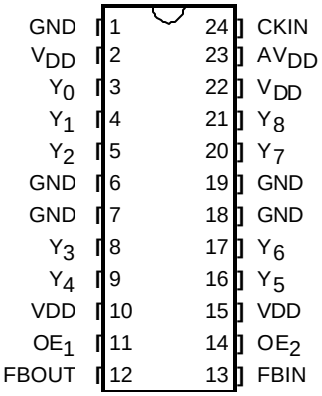
Each device has both a digital power supply signal (V_{DD}) and an analog power supply signal (V_{DDA}). The V_{DDA} signal is powered at same potential as V_{DD} during normal operation mode but can also be used as a test mode select signal. When V_{DDA} is forced to 0 V the PLL circuitry is bypassed and the CKIN input will be passed directly to the Y_n outputs without phase alignment. This mode has been provided for assistance to the device supplier in testing the device and is not intended for general usage by an end customer.

The devices are defined to operate between a 3.0 V to 3.6 V power supply range. The device is offered in a 24 thin shrink small outline package as defined in MO-153.

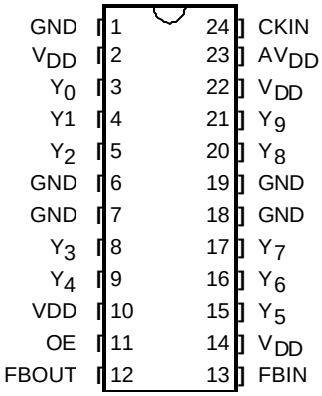
3 Device standard (cont'd)

3.2 Pinout figure

2509 Pin Assignment for 24 TSSOP



2510 Pin Assignment for 24 TSSOP



3.3 Terminal functions

Table 1 — Terminal function

Terminal name	Descriptions	Electrical characteristics
$1Y_0$-$1Y_4$ $2Y_0$-$2Y_3$	Clock Outputs for '2509	LV-CMOS
Y_0-Y_9	Clock Outputs for '2510	LV-CMOS
FBOUT	Clock Output used to provided the feedback reference for the PLL. Not affected by the OE Pins	LV-CMOS
CKIN	Reference Clock Input	LV-CMOS
FBIN	Feedback input to the PLL. The user connects this to the FBOUT signal.	LV-CMOS
OE_1, OE_2, OE	Output Enable Signals.	LV-TTL
V_{DDA}	Analog Power Supply for the PLL. Signal can also be used to shutoff and Bypass the PLL.	3.3 V Nominal
V_{DD}	Positive Supply Voltage	3.3 V Nominal
GND	Ground	Ground Supply

3 Device standard (cont'd)

3.3 Terminal functions (cont'd)

Table 2A — '2509 function table

Inputs				Outputs			Notes
OE_1	OE_2	CKIN	V_{DDA}	$1Y_0$-$1Y_4$	$2Y_0$-Y_3	FBOUT	
X	X	L	H	L	L	L	Normal Mode: V_{DDA} = H Outputs are phase locked to CKIN signal.
L	L	H	H	L	L	H	
L	H	H	H	L	H	H	
H	L	H	H	H	L	H	
H	H	H	H	H	H	H	
X	X	L	L	L	L	L	Test Mode: V_{DDA} = L PLL and VCO Disabled. Outputs are delayed with-respect-to the CKIN signal.
L	L	H	L	L	L	H	
L	H	H	L	L	H	H	
H	L	H	L	H	L	H	
H	H	H	L	H	H	H	
L = Logic LOW H = Logic HIGH X = Don't Care (But not floating)							

Table 2B — '2510 function table

Inputs			Outputs		Notes
OE	CKIN	V_{DDA}	Y_9-Y_0	FBOUT	
X	L	H	L	L	Normal Mode: V_{DDA} = H Outputs are phase locked to CKIN signal.
L	H	H	L	H	
H	H	H	H	H	
X	L	L	L	L	Test Mode: V_{DDA} = L PLL and VCO Disabled. Outputs are delayed with-respect-to the CKIN signal.
L	H	L	L	H	
H	H	L	H	H	
L = Logic LOW H = Logic HIGH X = Don't Care (But not floating)					

3 Device standard (cont'd)

3.5 Logic diagrams

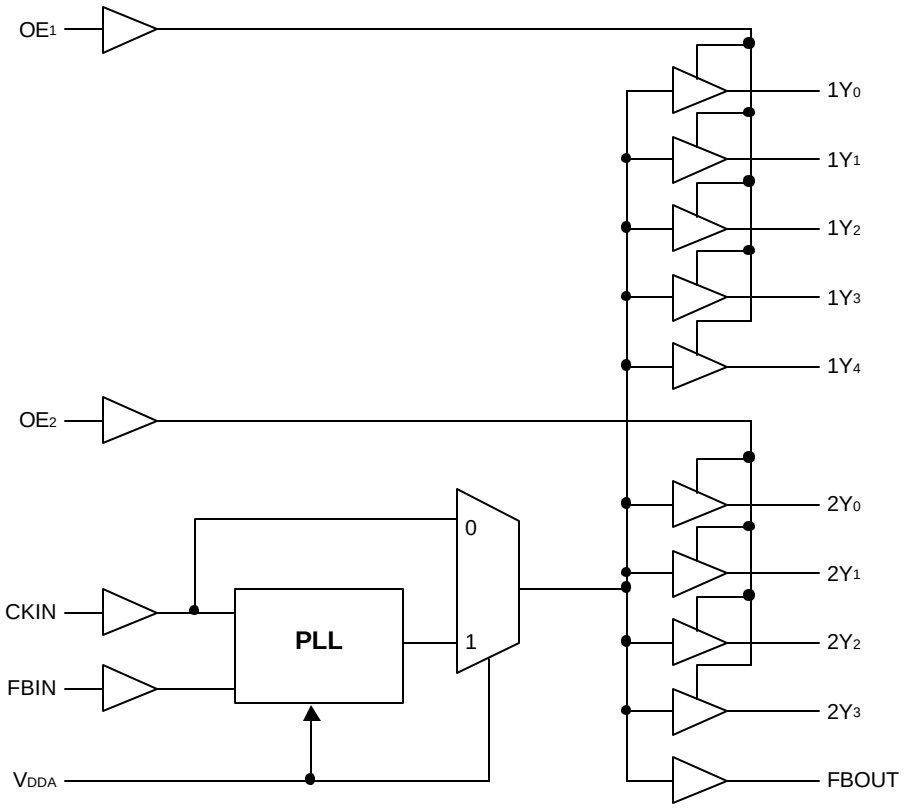


Figure 2A — '2509 PLL logic diagram (positive logic)

3 Device standard (cont'd)

3.5 Logic diagrams (cont'd)

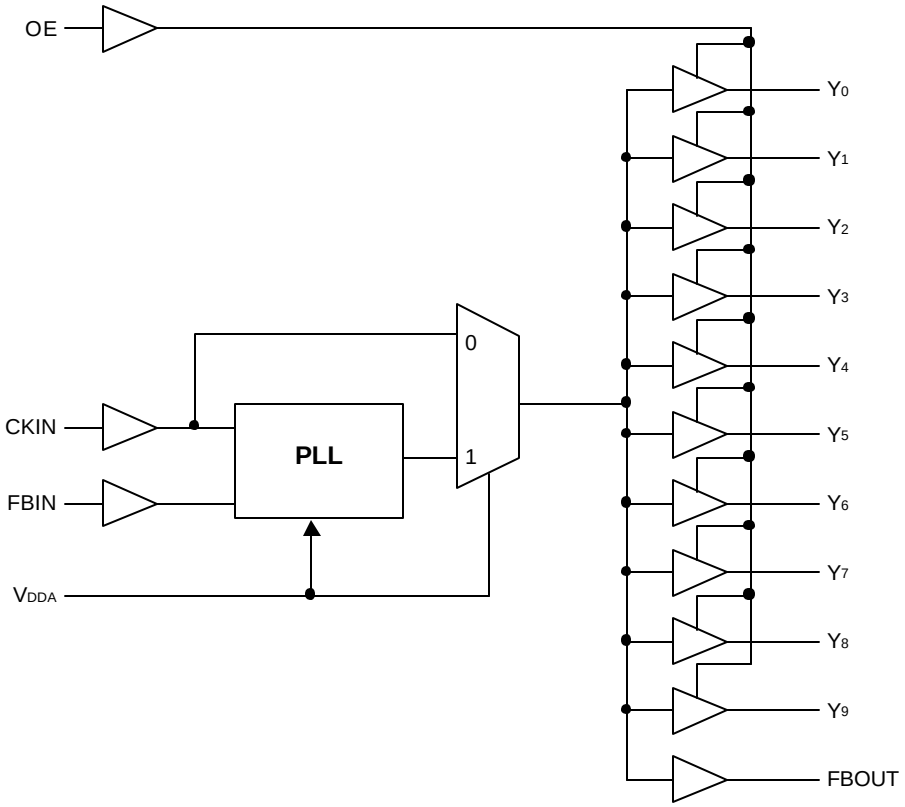


Figure 2B — '2510 Logic diagram (positive logic)

3.6 Absolute maximum ratings

Table 3 — Absolute maximum ratings

Supply voltage range, (V_{DD})	-0.5 V to 4.6 V
Supply voltage range (V_{DDA})	-0.5 V to 4.6 V
DC Input voltage range, (V_I)	-0.5 V to 4.6 V
DC Output voltage range (V_O)	-0.5 V to 4.6 V
Input clamp current (I_{IK})	-50 mA
Output clamp current (I_{OK})	±50 mA
Storage temperature range (T_{STG})	-65 ºC to 150 ºC
V_{DD}, GND current / pin (I_{DD} or I_{GND})	100 mA

NOTE 1 Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under these conditions is not implied.

NOTE 2 Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

3 Device standard (cont'd)

3.7 Recommended operating conditions

Table 4 — Recommended operating conditions

Symbol	Parameter	Standard range			Units
		Min	Typ	Max	
V_{DD}	Supply voltage	3.0	3.3	3.6	V
V_{DDA}	Analog supply voltage	3.0	3.3	3.6	V
V_{IN}	Voltage Applied to input pins	0		V_{DD}	V
I_{OH}	High-level output current			-12	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	ºC
D_{tin}	Input Duty Cycle	40%		60%	

3.8 DC specifications

Table 5 — DC specifications

Symbol	Parameter	Condition	T_A = 0 °C to 70 °C V_{DD} = 3.3 V ±0.3 V			Units
			Min	Typ	Max	
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW level input voltage				0.8	V
V_{OH}	HIGH-level output voltage	I_{OH} = -12 mA, V_{IH} = 2.0 V V_{DD} = 3.0 V	2.1			V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA, V_{IL} = 0.8 V V_{DD} = 3.0 V			0.8	
I_I	Input leakage current	V_I = V_{DD} or GND			±10.0	µA
I_{DD}	Quiescent Supply Current	V_I = V_{DD} or GND, I_O = 0				µA

3.9 Timing requirements

Table 6 — AC specifications

Symbol	Parameter	Condition	T_A = 0 °C to 70 °C V_{DD} = 3.3 V ±0.3 V			Units
			Min	Typ	Max	
Dt	Duty Cycle	Figures 2, 8	45%		55%	
	Output Slew Rate	See figures 1, 3			Note 1	V/ns
tphl	Disable Time OE to Yn	See figures 1, 4			Note 1	ns
NOTE 1 Should be specified by vendor for completeness.						

3 Device standard (cont'd)

3.10 AC specifications

Table 7 — Critical PLL specifications

Symbol	Parameter	Conditions	T_A = 0 to 70 °C V_{DD} = 3.3 V ±0.3 V			Units
			Min	Typ	Max	
f_{OP}	Operating Frequency		50		140	MHz
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	See Figures 2, 5	-75		+75	ps
t_{SSC}	SSC Induced Skew NOTES 1 & 2				150	ps
$t_{SK(O)}$	Output to Output Skew	See Figures 2, 7			150	ps
C_{IN}	Clock Input Capacitance			4.0		pF
t_ϕ	Static Phase Offset	See Figures 2, 6	-150		+150	ps
C_{FB}	Feedback Capacitor Value	See Figure 2	Note 3		Note 3	pF

NOTE 1 SSC = Spread Spectrum Clock. The use of SSC synthesizers on the system motherboard will reduce EMI.

NOTE 2 Skew is defined as the total clock skew between any two outputs and is therefore specified as a maximum only.

NOTE 3 Individual Vendor Value needs to be specified for proper operation of the PLL.

3.11 Spread Spectrum Specifications (SSC)

The PLL used on registered DIMM needs to support SSC synthesizers with the parameters listed in Table 8.

Table 8 — Spread Spectrum Specifications

Parameter	Min	Max
Modulation Frequency	30 kHZ	50 kHz
Clock Frequency Deviation Downspread (For 133 MHz: 132.5 to 133 MHz range)	0 %	0.5 %
PLL designs should target the following values to meet the 150 ps maximum of SSC induced skew: • Greater than 1.2 MHz PLL loop bandwidth • Less than -0.031 degrees of phase angle		

4 Test Circuit and switching waveforms

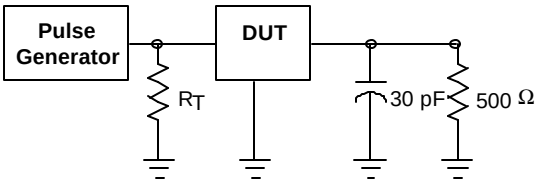


Figure 1 — Test circuit

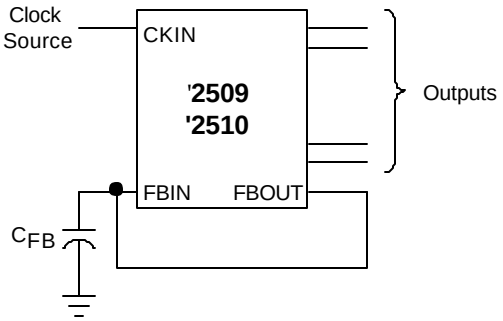


Figure 2 — Application test circuit

Test circuit component values

R_L = Load Resistor

C_L = Load Capacitance, includes parasitics

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generator

C_{FB} = PLL Feedback Capacitance.

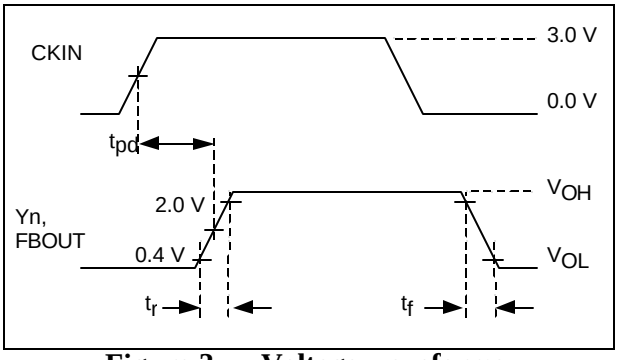


Figure 3 — Voltage waveforms
Propagation delay times during test mode

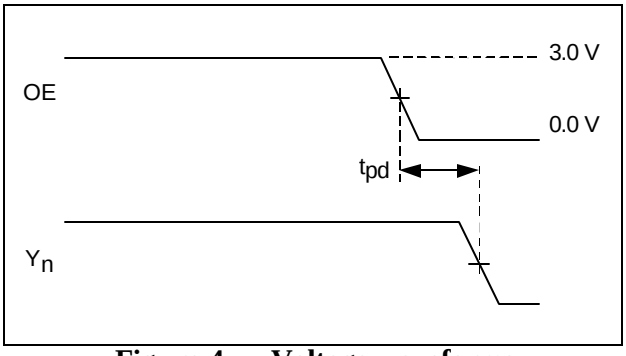


Figure 4 — Voltage waveforms
OE disable times

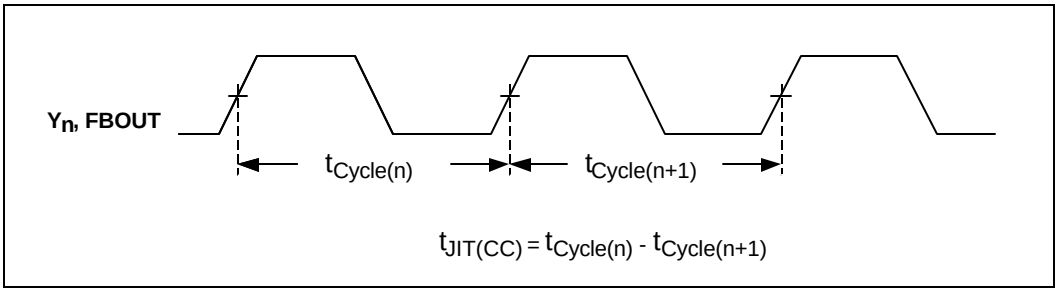


Figure 5 — Cycle-to-cycle jitter

4 Test Circuit and switching waveforms (cont'd)

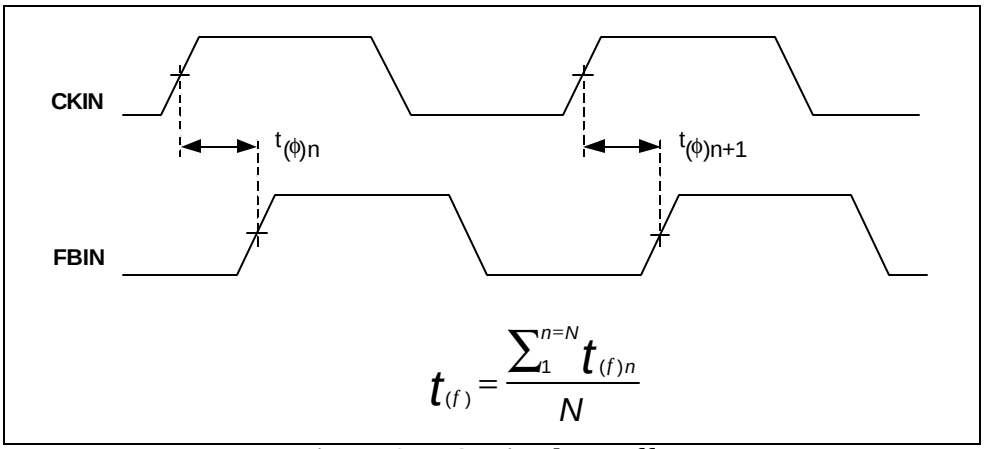


Figure 6 — Static phase offset

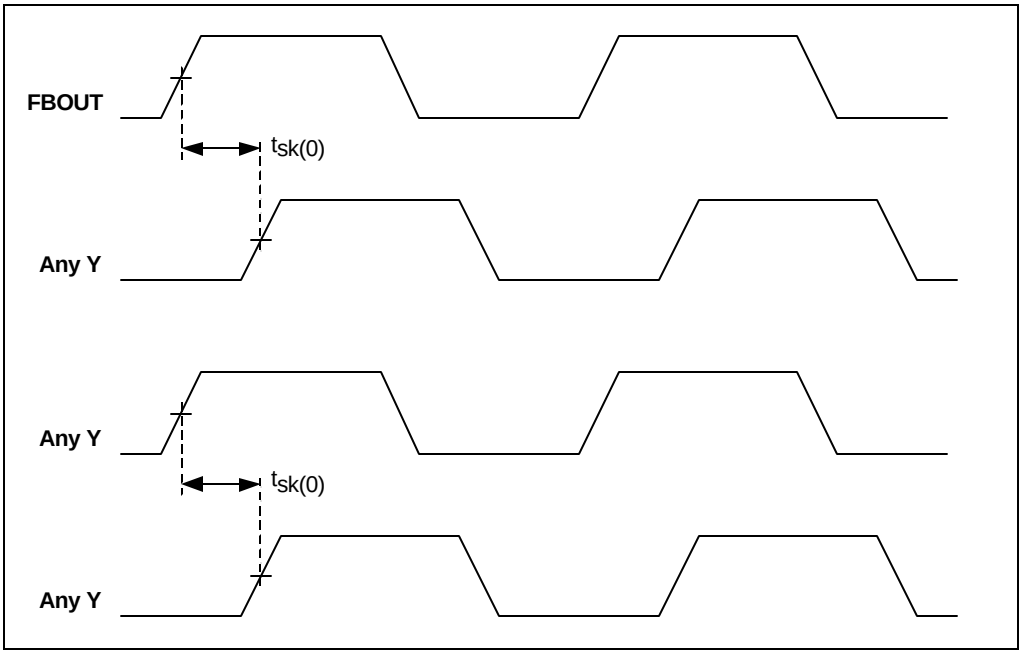


Figure 7 — Output skew

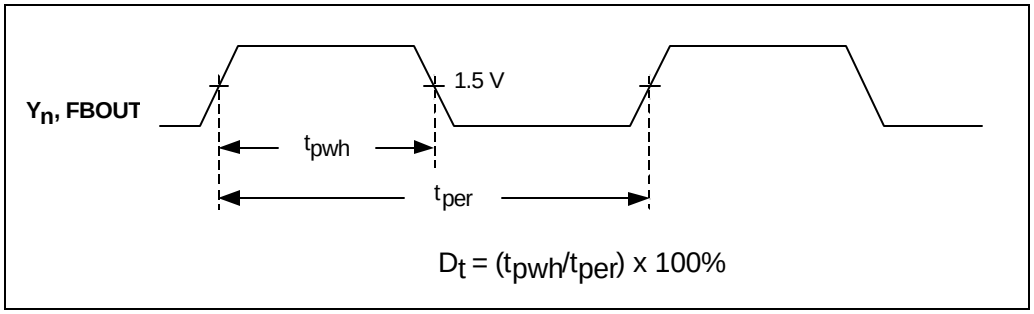


Figure 8 — Duty cycle

5 Reference to other applicable JEDEC standards and publications

JESD52, *Standard for Description of Low Voltage TTL-Compatible CMOS Logic Devices*

JESD65, *Definition of Skew Specification for Standard Logic Devices*

JESD21-C, *Configuration for Solid State Memories*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